

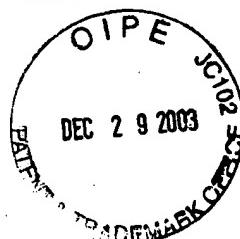
DEC. 18 2003



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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/664,210	09/17/2003	2812	1326	CS01-208	3	52	3



GEORGE O. SAILE  
 28 DAVIS AVENUE  
 POUGHKEEPSIE, NY 12603

CONFIRMATION NO. 3897

## FILING RECEIPT



\*OC000000011493188\*

Date Mailed: 12/15/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

## Applicant(s)

Yong Meng Lee, Singapore, SINGAPORE;  
 Da Jin, Singapore, SINGAPORE;  
 Tommy Mau Lam Lai, Singapore, SINGAPORE;  
 David Vigar, Singapore, SINGAPORE;  
 Siow Lee Schwa, Singapore, SINGAPORE;

Chua

## Domestic Priority data as claimed by applicant

## Foreign Applications

If Required, Foreign Filing License Granted: 12/13/2003

Projected Publication Date: 03/17/2005

Non-Publication Request: No

Early Publication Request: No

## Title

Method of forming double-gate semiconductor-on-insulator (SOI) transistors

## Preliminary Class

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Title 35, United States Code, Section 184  
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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December 18, 2003

To: Commissioner for Patents  
Mail Stop Application Number  
Customer Service Center  
P.O. Box 1450  
Alexandria, VA 22313-1450

From: Stephen B. Ackerman

Subject: Serial No.: 10/664,210  
Filing Date: 09/17/03  
Inventor: Y. M. Lee, et al  
Title: Method of Forming Double-Gate Semiconductor-On-Insulator (SOI) Transistors

**REQUEST TO CORRECT FILING RECEIPT**

Dear Sir:

On the copy of the enclosed Filing Receipt, there are errors in the list of Applicants. The fifth Applicant's name is misspelled. Mr. Chwa's corrected name and residence reads; **Siow Lee Chwa, Singapore, Singapore.**

Please make the necessary change to correct the error on the Filing Receipt.

If there are any questions, please contact the undersigned attorney at (845) 452-5863. Thank you for your attention to this matter.

Respectfully Submitted,



Stephen B. Ackerman, Reg. No. 37,761